Remarks

Claims 1-5, 10-14, and 18-20 remain pending in the present application. Claims 6-9 and 15-17 were previously canceled in response to a restriction requirement. The Applicants respectfully request reconsideration of the above captioned patent application in light of the remarks presented herein.

Allowable Material

Claims 10-14 are indicated to be allowable.

Claims 2, 3, 19 and 20 are indicated to be allowable if rewritten in independent form including all of the limitations of the base claims and any intervening claims.

Applicants thank the Examiner for indicating allowable material.

35 USC § 102

Claims 1, 4, 5 and 18 stand rejected under 35 USC § 102(b) as being allegedly unpatentable over Yamamoto et al. (US 5,444,744, "Yamamoto"). Applicants have reviewed the cited reference and respectfully assert that embodiments in

accordance with the present invention as recited in Claims 1, 4, 5 and 18 are patentable over Yamamoto.

With regard to Claim 1, Applicants respectfully assert that Yamamoto fails to teach or fairly suggest the limitation "a stream of reset pulses" as recited by Claim 1. Applicants respectfully assert that one of ordinary skill in the art would understand the instant limitation as requiring a stream of pulses that cause a resetting action.

The rejection alleges that output signal "B" from Yamamoto item 15 suggests the recited "stream of reset pulses" as recited by Claim 1. Applicants respectfully traverse. Yamamoto teaches, "[a] D-FF (Flip-Flop) is utilized as the multiplier 11 which samples the input signal A supplied to the D-input terminal at the timings of the reference signal B supplied to the CK-input terminal" (column 6 lines 32-35). Herein, Yamamoto clearly teaches that the "B" signal is "supplied to the CK (clock) input terminal," not to a reset terminal. Further, Yamamoto clearly teaches the function of the "B" signal is to "sample() the input signal A supplied to the D-input terminal at the timings of the reference signal B." Thus, the "B" signal latches the input signal A, does not perform a reset function, and is not a reset signal.

Moreover, no signal described in Yamamoto can fairly be described as a reset signal, and no device or circuit block described in Yamamoto is taught to have a reset input.

Consequently, as Yamamoto fails to teach or fairly suggest the limitation "a stream of reset pulses" as recited by Claim 1, Applicants respectfully assert that Claim 1 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

In addition with respect to Claim 1, Applicants respectfully assert that Yamamoto fails to teach or fairly suggest "a pass/fail indicator signal as a function of said stream of reset pulses and a difference between an input signal and a reference voltage" as recited by Claim 1. Even if, *arguendo*, signal "B" can be construed as the recited stream of reset pulses, there is no signal illustrated in Yamamoto that teaches or fairly suggests the recited "pass/fail indicator signal."

The rejection alleges that Yamamoto signal "E" suggests the recited "pass/fail indicator signal" as recited by Claim 1. Applicants respectfully traverse. Item 9 is an analog to digital converter. While Yamamoto is silent as to the resolution of the A/D converter, Yamamoto does illustrate that it is limited to outputting only a single bit at a time. Figure 9A shows its output to be a pulse stream, e.g., alternating high and low levels. No single level of the waveform 9A can be said to represent a difference between "an input signal and a reference voltage" as recited by Claim 1. Consequently, any signal deriving from "A" cannot teach the recited "pass/fail indicator signal" as recited by Claim 1.

For this additional reason, Applicants respectfully assert that Claim 1 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

Moreover, inspection of waveform 9E, corresponding to signal "E" and alleged by the rejection to suggest the instant limitation, shows that signal "E" is not the recited "pass/fail indicator signal" as recited by Claim 1. For example, when 9A is low for the first time, 9E is both high and low. Consequently, for the same analog input, and therefore the same "difference between an input signal and a reference voltage," signal E provides both a high and a low indication. Applicants respectfully assert that a signal that is high and low for the same "difference between an input signal and a reference voltage" is not and cannot teach or fairly suggest the recited "pass/fail indicator signal" as recited by Claim 1.

For this yet additional reason, Applicants respectfully assert that Claim 1 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

Further with respect to Claim 1, Applicants respectfully assert that Yamamoto does not teach or fairly suggest "an event of said pass/fail indicator is correlated to a specific period of said clock signal at which said event occurred" as recited by Claim 1. Applicants respectfully note that the rejection fails to even allege that Yamamoto suggests this limitation, as the rejection omits the term "specific" from its allegation.

Applicants respectfully assert that, even if, *arguendo*, Yamamoto suggests, "a correlation module having a first correlation input for receiving said clock signal, a second correlation input communicatively coupled to said indicator output of said indicator module, wherein an event of said pass/fail indicator is correlated to a period of said clock signal at which said event occurred" as alleged in the rejection, such suggestion fails to teach or fairly suggest the limitation recited in Claim 1. The instant limitation recites correlation to a "specific period of said clock signal." Applicants respectfully assert that Yamamoto is void of any teaching to identify a "specific period" as recited by Claim 1.

For this further reason, Applicants respectfully assert that Claim 1 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

Moreover, Yamamoto cannot teach or fairly suggest correlation of "an event of said pass/fail indicator ... to a specific period of said clock signal at which said event occurred" as recited by Claim 1. Since item 9 is an analog to digital converter that outputs a pulse stream, any change to the input of item 9 is not reflected in its output stream for some period of time, related to conversion time and output cycle. Hence, some non-zero number of clock signals "B" must occur before any possible indication of the change has propagated through the rest of the circuit. Consequently, correlation to the specific period of the clock signal, as recited by Claim 1, is not taught or suggested.

For this still further reason, Applicants respectfully assert that Claim 1 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

The rejection argues that clock "J" (indicated on Office-supplied copy of Figure 8) correlates to an event of the recited pass/fail indicator. Applicants respectfully assert that a specific period of clock "J" cannot be correlated to an event of the recited pass/fail indicator, as periods of clock "J" are lost in variable divider 15b, in producing signal "B" which latches signal "A." For example, if 15b divides by ten, then signal "A" is only latched every ten periods of signal "J." Consequently, the alleged pass/fail indicator "E" does not have the same resolution as signal "J." Hence, "E" cannot correlate with any period of "J" as alleged by the rejection.

For this still yet further reason, Applicants respectfully assert that Claim 1 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

Applicants respectfully assert that Claims 2-5 are allowable as they depend from an allowable base claim, and respectfully solicit allowance of these Claims.

Applicants respectfully assert that Claim 18 overcomes the rejections of record for at least the rationale previously presented with respect to Claim 1. Applicants respectfully reiterate that Yamamoto is void of any teaching to identify a "specific period" as recited by Claim 18.

CONCLUSION

Claims 1-5, 10-14, and 18-20 remain pending in the present application. The Applicants respectfully request reconsideration of the above captioned patent application in light of the remarks presented herein.

The Examiner is invited to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Please charge any additional fees or apply any credits to our PTO deposit account number: 23-0085.

Respectfully submitted,

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